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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,150	10/26/2001	Hung T. Nguyen	01-621	3566

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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,150	NGUYEN, HUNG T.	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. This application lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 6, 7, 8, 10, 13, 14, 15, 17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al, US Patent 5,784,603, in view of Arizono US Patent 4,910,664.

5. Referring to claim 1, Leung et al. have taught for use is a processor having an external memory interface, an instruction prefetch mechanism, comprising:

a. a branch predictor that predicts whether a branch is to be taken (Figure 1, element 32, column 3, lines 55-56);

b. prefetch circuitry, coupled to said branch predictor, that prefetches instructions associated with said branch via said external memory interface if said branch is taken and

prefetches sequential instructions via said external memory interface if said ranch is not taken (Figure, element 30, column 7, lines 2-32, column 3, line 35-column 4, line 63).

6. Leung et al. have not specifically taught a loop recognizer, coupled to said prefetch circuitry, that determines whether a loop is present in fetched instructions an reinstates a validity of instructions in said loop and prevents said prefetch circuitry from prefetching instructions outside of said loop until said loop completes execution.

7. However, Arizono has taught a loop recognizer, coupled to said prefetch circuitry, that determines whether a loop is present in fetched instructions an reinstates a validity of instructions in said loop and prevents said prefetch circuitry from prefetching instructions outside of said loop until said loop completes execution (abstract, column 3, lines 8-67) for the desirable purpose of avoiding wasteful prefetching (column 6, lines 50-55). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Leung et al., include the claimed loop recognizer, as taught by Arizono, for the desirable purpose of avoiding wasteful prefetching (column 6, lines 50-55).

8. Referring to claim 3, Leung et al. have taught the mechanisms recited in claim 1, as described above, and wherein said prefetch circuitry prefetches four of said instructions at a time (column 3, lines 49-53).

9. Referring to claim 6, Leung et al. have taught the mechanism as recited in claim 1, as described above, and wherien said prefetch circuitry is embodied in a state machine (Figure, element 30, column 7, lines 2-32, column 3, line 35-column 4, line 63).

10. Referring to claim 7, Leung et al. have taught the mechanism as recited in claim 1, as described above, and wherein said processor is a digital signal processor (Leung et al, Figure 1).

11. Claim 8 does not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.

12. Claim 10 does not recite limitations above the claimed invention set forth in claim 3 and is therefore rejected for the same reasons set forth in the rejection of claim 3 above.

13. Claim 13 does not recite limitations above the claimed invention set forth in claim 6 and is therefore rejected for the same reasons set forth in the rejection of claim 6 above.

14. Claim 14 does not recite limitations above the claimed invention set forth in claim 7 and is therefore rejected for the same reasons set forth in the rejection of claim 7 above.

15. Referring to claim 15, Leung et al. have taught a digital signal processor, comprising:

a. an execution core having an instruction cache (Figure 1, element 24);

b. a memory unit coupled to said execution core and having an instruction memory (column 3, lines 57-60) and an external memory interface (Figure 1, element 36);

c. a branch predictor, coupled to said instruction cache, that predicts whether a branch is to be taken (Figure 1, element 32, column 3, lines 55-56);

d. prefetch circuitry, coupled to said branch predictor, that prefetches instructions associated with said branch via said external memory interface if said branch is taken and prefetches sequential instructions via said external memory interface if said ranch is not taken (Figure, element 30, column 7, lines 2-32, column 3, line 35-column 4, line 63).

16. Leung et al. have not specifically taught a loop recognizer, coupled to said prefetch circuitry, that determines whether a loop is present in fetched instructions an reinstates a validity of instructions in said loop and prevents said prefetch circuitry from prefetching instructions outside of said loop until said loop completes execution.

17. However, Arizono has taught a loop recognizer, coupled to said prefetch circuitry, that determines whether a loop is present in fetched instructions an reinstates a validity of instructions in said loop and prevents said prefetch circuitry from prefetching instructions outside of said loop until said loop completes execution (abstract, column 3, lines 8-67) for the desirable purpose of avoiding wasteful prefetching (column 6, lines 50-55). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Leung et al., include the claimed loop recognizer, as taught by Arizono, for the desirable purpose of avoiding wasteful prefetching (column 6, lines 50-55).

18. Claim 17 does not recite limitations above the claimed invention set forth in claim 3 and is therefore rejected for the same reasons set forth in the rejection of claim 3 above.

19. Claim 20 does not recite limitations above the claimed invention set forth in claim 6 and is therefore rejected for the same reasons set forth in the rejection of claim 6 above.

20. Claims 2, 9, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al, US Patent 5,784,603, in view of Arizono US Patent 4,910,664, and Bogin et al., US Patent 5,835,435.

21. Referring to claim 2, Leung et al. have taught the mechanism as recited in claim 1, as described above. Leung et al. have not specifically taught wherein said external memory interface is a synchronous memory interface. However, Bogin et al. have taught that data can be read from or written to sequential addresses in synchronous memory, or DRAM, significantly faster than in other types of memory (Bogin et al., column 1, lines 13-33). Therefore it would have obvious to one of ordinary skill in the art at the time the invention was made to have the

memory interface be a synchronous memory interface, or DRAM, for the desirable purpose quickly accessing addresses in the memory (Bogin et al., column 1, lines 13-33).

22. Claim 9 does not recite limitations above the claimed invention set forth in claim 2 and is therefore rejected for the same reasons set forth in the rejection of claim 2 above.

23. Claim 16 does not recite limitations above the claimed invention set forth in claim 2 and is therefore rejected for the same reasons set forth in the rejection of claim 2 above.

24. Claims 4, 11, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al, US Patent 5,784,603, in view of Arizono US Patent 4,910,664, and Chi, US Patent 6,243,807.

25. Referring to claim 4, Leung et al. have taught the mechanism as recited in claim 1 as described above. Leung et al. have not specifically taught wherein said prefetch circuitry causes said instructions to be placed in a direct mapped instruction cache in said processor. However, Chi has taught placing instructions in a direct mapped instruction cache in order to reduce the execution time for looped routines (Chi, column 8, lines 38-46). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to place the instructions of Leung et al., into a direct mapped instruction cache, as taught by Chi, for the desirable purpose of reducing the execution time of looped routines (Chi, column 8, lines 38-46).

26. Claim 11 does not recite limitations above the claimed invention set forth in claim 4 and is therefore rejected for the same reasons set forth in the rejection of claim 4 above.

27. Claim 18 does not recite limitations above the claimed invention set forth in claim 4 and is therefore rejected for the same reasons set forth in the rejection of claim 4 above.

28. Claims 5, 12, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al, US Patent 5,784,603, in view of Arizono US Patent 4,910,664, and Tokuume, US Patent 4,965,722.

29. Referring to claim 5, Leung et al. have taught the mechanism as recited in claim 1, as described above. Leung et al. have not taught wherein said prefetch circuitry drives a request arbiter in said processor. However, Tokuume has taught a prefetch circuitry that drives a request arbiter (Tokuume, column 3, lines 1-25) in order to select and grant priority to a signal when more than one signal is received (Tokuume, column 3, lines 1-25). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the prefetch circuitry of Leung et al., drive a request arbiter in the processor, for the desirable purpose of selecting and granting priority to a signal when more than one signal is received (Tokuume, column 3, lines 1-25).

30. Claim 12 does not recite limitations above the claimed invention set forth in claim 5 and is therefore rejected for the same reasons set forth in the rejection of claim 5 above.

31. Claim 19 does not recite limitations above the claimed invention set forth in claim 5 and is therefore rejected for the same reasons set forth in the rejection of claim 5 above.

Conclusion

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 8-4:30.

33. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

34. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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